WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a substrate having a top surface;

a first dielectric layer formed above the substrate having a trench formed therein, the first dielectric layer having a first dielectric constant;

a first metal layer formed within the trench of the first dielectric layer;

a second dielectric layer formed above the first metal layer and having a trench formed therein, the second dielectric layer having a second dielectric constant;

a second metal layer formed within the trench of the second dielectric layer;

a third dielectric layer formed above the second metal layer and having a trench formed therein, the third dielectric layer having a third dielectric constant; and

a third metal layer formed within the trench of the third dielectric layer.

2. The integrated circuit of claim 1 wherein said first dielectric layer has a dielectric constant of less than 2.8, said second dielectric layer has a dielectric constant of between 2.8 and 3.3, and said third dielectric layer has a dielectric constant of above 3.0.

3. The integrated circuit of claim 1 wherein said first dielectric layer comprises a material selected from the group consisting of an oxide and methylsilsesquioxane ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid.

4. The integrated circuit of claim 1 wherein said second dielectric layer comprises a material selected from the group consisting of an oxide and methylsilsesquioxane

("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid .

5. The integrated circuit of claim 1 wherein said third dielectric layer comprises a material selected from the group consisting of silicon glass, undoped silicon glass, fluorine doped silicon glass, and high-density chemical vapor deposition (HPVCD) silicon oxide.

6. The integrated circuit of claim 1 further comprising a first transistor and a second transistor formed within the substrate and wherein the first and second transistors are electrically coupled through the metal layers.

7. A method of forming an integrated circuit comprising:

forming a transistor within a substrate;

depositing a first dielectric material over the transistor;

forming an opening to the transistor in the first dielectric material;

depositing a first metal pattern within the first dielectric material;

depositing a second dielectric material, having a higher dielectric constant than the first dielectric material, over the first metal pattern;

forming an opening to the first metal pattern in the second dielectric material;

depositing a second metal pattern within the second dielectric material;

depositing a third dielectric material, having a higher dielectric constant than the first and second dielectric materials, over the second metal pattern;

forming an opening to the second metal pattern in the third dielectric material; and

depositing a third metal pattern in the third dielectric material.

8. The method of claim 7 wherein depositing a first dielectric material comprises spin-on depositing a material having a dielectric constant of below 2.8, depositing a second dielectric material comprises spin-on depositing a material having a dielectric constant of between 2.5 and 3.3, and depositing a third dielectric material comprises spin-on depositing a material having a dielectric constant of above 3.0.

9. The method of claim 7 further comprising depositing a fourth dielectric material, having a higher dielectric constant that is different than the first, second, and third dielectric materials, over the third metal pattern.

10. The method of claim 7 wherein depositing a first dielectric material comprises depositing a material selected from the group consisting of an oxide and methylsilsesquioxane ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid.

11. The method of claim 10 wherein depositing a second dielectric material comprises depositing a material selected from the group consisting of an oxide and methylsilsesquioxane ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid.

12. An electrical device comprising:

a plurality of metal layers formed one atop the other;

a plurality of inter-level dielectric layers, each such inter-level dielectric layer serving to electrically insulate at least one metal layer from at least one other metal layer;

wherein the plurality of inter-level dielectric layers includes:

at a lower region, inter-level dielectric layers having a first dielectric constant,

at a middle region, inter-level dielectric layers having a second dielectric constant; and

at an upper region, inter-level dielectric layers having a third dielectric constant.

13. The electrical device of claim 12 wherein:

the first dielectric constant is below 2.8;

the second dielectric constant is between 2.5 and 3.3; and

the third dielectric constant is above 3.0.

14. The electrical device of claim 12 wherein the lower region inter-level dielectric layer comprises a material selected from the group consisting of an oxide and methylsilsesquioxane ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid .

15. The electrical device of claim 12 wherein the middle region inter-level dielectric layer comprises a material selected from the group consisting of an oxide and

methylsilsesquioxane ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, and a porogen / HSQ hybrid.

16. The electrical device of claim 12 wherein the upper region inter-level dielectric layer comprises a material selected from the group consisting of undoped silicon glass, doped silicon glass, and silicon oxide.

17. The electrical device of claim 12 wherein the first dielectric constant is lower than the second and third dielectric constants.

18. The electrical device of claim 12 wherein the second dielectric constant is lower than the first and third dielectric constants.

19. An integrated circuit comprising:

a substrate;

a plurality of transistors formed on the substrate;

a plurality of isolation regions electrically isolating at least one of the plurality of transistors from at least one other of the transistors;

a first dielectric layer, having a first dielectric constant, formed above the substrate having formed therein a via to a transistor, and an interconnect structure;

a second dielectric layer, having a second dielectric constant, formed above the first dielectric layer and having formed therein a second interconnect structure; and

a third dielectric layer, having a third dielectric constant, formed above the second dielectric layer and having formed therein a third interconnect structure.

20. The integrated circuit of claim 19 wherein the transistors have gate lengths of 130 microns or less.

21. The integrated circuit of claim 19 wherein the substrate is a silicon-on-insulator substrate.

22. The integrated circuit of claim 19 wherein the first and second dielectric layers comprise a material selected from the group consisting of an oxide and methylsilsesquioxane ("MSQ") hybrid, an MSQ derivative, porogen/MSQa hybrid, an Oxide / Hydrogen silsesquioxane ("HSQ") hybrid, an HSQ derivative, a porogen / HSQ hybrid, nanoporous silica, xerogel, and Poly tetra fluoro ethylene ("PTFE").

23. The integrated circuit of claim 19 further comprising a first insulator layer between the substrate and the first dielectric layer.

24. The integrated circuit of claim 19 wherein the via connects to a doped region of a transistor.

25. The integrated circuit of claim 19 wherein the second dielectric constant is lower than the third dielectric constant and the first dielectric constant is lower than both the second and third dielectric constants.